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PCO

THE GROWTH OF EPITAXIAL GaAs AND GaAlAs ON SILICON SUBSTRATES BY MOVPE

PROJECT NO: N00014-86-C-2432

FINAL REPORT

MARCH 1990

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CONTENTS

1. INTRODUCTION

This is the final report on the project which covers, in detail, the work carried out in the period 1 June to 31 August 1989, and summarises the overall achievements of the project from September 1986 to September 1989.

1.1 OBJECTIVE

The objectives of the programme were to undertake research into the growth of GaAs and AlGaAs on silicon substrates, to refine deposition techniques, and optimise the electrical, optical, and structural properties of the layers; to prepare GaAs/AlGaAs heterostructures on silicon for opto-electronic and microwave devices; and to explore the monolithic integration of III-V devices on silicon CMOS ICs.

1.2 PROJECT OVERVIEW

All the major objectives of the programme have been pursued and some important achievements are summarised below. These are discussed in more detail in Section 4. In Section 5, we draw some conclusions and make recommendations for future activities in GaAs on silicon.

We suggest a way forward for the achievement of a CMOS compatible Si/GaAs based OEIC process.

1.2.1 Summary of Achievements

We have made substantial achievements within the area of materials growth, resulting in the development of a successful process for the MOVPE growth of GaAs onto silicon substrates. This success has enabled the demonstration of several excellent device results. In the two sections below, our device and materials growth achievements are outlined.

(i) Devices

(a) GaAs on silicon MESFETs have been demonstrated with performance equivalent to homo-epitaxial devices. An impressive transconductance figure of 180mSmm^{-1} was achieved for a 0.7μm gate length.

(b) GaInAs photodetectors grown onto patterned silicon substrate have displayed excellent device characteristics. Devices with leakage current densities of $1.3 \times 10^{-4} Acm^{-2}$ at -5V bias with an external uncoated quantum of efficiency of 59% at 1.3μm have been demonstrated.

(c) GaAlAs/GaAs HBT devices on a 3" silicon wafer have been demonstrated. Optimisation of device doping characteristics would allow their performance to be improved.

(d) LEDs and LASERs have been fabricated. These devices, as expected, had their performance limited by the high threading dislocation density inherent in this materials system.

(ii) Materials Growth

(a) Development of substrate surface preparation techniques to give reproducible GaAs on silicon epitaxy free from anti-phase boundaries.

(b) Investigation of initial layer growth and in-situ annealing resulting in a layer of homogeneous strain distribution and low misfit twin and stacking fault density.

c) Investigation of the relationship between substrate orientation and layer quality.

(d) Selective area epitaxy for

(i) growth in windows opened up in Si_3N_4 or SiO_2 masks
(ii) on mesas with V-groove channel isolation

(e) Investigation of low temperature substrate cleaning, including the use of external microwave and in-situ RF induced plasmas.

(f) Development and careful calibration of a chemical defect revealing etch and optical microscopy to assess material quality.

(g) Threading dislocation reduction by the use of GaInAs/GaAs SLS dislocation filters and GaAs spacer layers. This has enabled dislocation densities to be reduced to $\sim 10^7 cm^{-2}$ for vicinal (001) wafers.

(h) Development of a potential scheme for opto-electronic integration with silicon CMOS.

1.3 PLANNED WORK FOR QUARTER 12

(a) Continue low temperature silicon cleaning experiments.

(b) Continue experiments aimed at materials improvement by combination of cyclic thermal annealing (CTA), strained layer superlattices (SLS), and growth on profiled substrates.

(c) Selective area epitaxy.

(d) Growth of InP on silicon.

1.4 SUMMARY OF PROGRESS IN QUARTER 12

1.4.1 Low Temperature Silicon Cleaning

Low temperature silicon cleaning experiments were continued during quarter 12. Key parameters which have been identified as influencing the low temperature cleaning of silicon are: chemical pre-treatment, gas composition during cleaning, reactor pressure, substrate temperature, substrate orientation, plasma conditions, and duration of the cleaning treatment.

Successful substrate cleaning at temperatures down to 940^{0}C was demonstrated using hydrogen at a pressure of 100Torr. Plasma cleaning techniques were also explored in an attempt to achieve adequate substrate cleaning at lower temperatures down to 800^{0}C. Cleaning was found to be limited by the availability of active hydrogen at the substrate surface, and contamination of the plasma by reaction with the cell walls.

1.4.2 Combined Use of Cyclic Thermal Anneal (CTA), SLS and Profiled Substrates

This has been the main thrust of our growth experiments during this quarter. We have demonstrated very effective defect pinning at the edges of GaAs mesas isolated by 'V' groove channels in the silicon substrate. This material was grown using the CTA routines described in quarter 10, in conjunction with the use of 2 bands of GaInAs SLS.

Using these techniques, dislocation densities of $\sim 10^7 cm^{-2}$ were observed at the surface of the mesas. We have thus confirmed that this is a promising technique for achieving low dislocation densities in small areas of thin GaAs on silicon.

1.4.3 Selective Area Epitaxy (SAE)

Selective area epitaxy has been demonstrated as an effective method by which threading dislocation (TD) densities can be reduced. In quarter 11, we indicated that, at the process temperatures required for effective substrate cleaning, a contamination of the exposed substrate window could occur when using a substrate patterned with an oxide mask. We believe that this contamination occurs purely as a feature of the high process temperatures. At lower process temperatures, it has been demonstrated at Plessey Research that excellent quality silicon can be homo-epitaxially grown onto a masked silicon substrate.

Using atmospheric pressure MOVPE, there is no selectivity between the oxide and the substrate window. The Plessey process for the growth of GaAs on Si uses an aluminium containing layer to enhance the initial nucleation, exploiting stronger Si-Al bonding. The omission of this layer had no noticable effect upon mask to window selectivity. This suggests that polycrystalline to single crystal nucleation (ie mask to window), under the growth conditions employed, is not greatly influenced by the presence of a Si-Al bonding characteristic. This result confirms the suitability of using the aluminium containing layer in a selective area epitaxy process as it has no adverse effects in comparison to using a GaAs nucleation layer.

Enhanced dislocation filtering has been demonstrated by layers grown onto 'V' groove substrates. The observation of dislocation loss to the sidewalls (Section 3) and demonstration of improved residual threading dislocation densities by using selective area epitaxy brings the possibility of low threading dislocation (TD) density GaAs on Si closer to reality. The observations upon threading dislocations and recent develoments in low pressure/low temperature silicon homoepitaxial SAE at Plessey Research indicate that the future for the growth of GaAs on silicon by selective area epitaxy is very positive.

2. MATERIALS GROWTH

2.1 LOW TEMPERATURE SILICON CLEANING

2.1.1. Introduction

We aimed to establish the cleaning procedures and growth conditions under which high quality epitaxial growth could be achieved on silicon substrates which had been cleaned at low ($<900^0C$) temperatures.

Low temperature cleaning of silicon may be considered to be influenced by the following seven factors:

1. Chemical pre-treatment, or etching
2. Composition of the gas during cleaning
3. Gas pressure
4. Temperature
5. Crystallographic orientation
6. Duration of cleaning
7. Plasma conditions

The dependence of epitaxial layer quality on these factors has been systematically studied, the effect of substrate orientation and chemical pre-treatment orientation was assessed by simultaneously growing on two or three substrates of different orientation and/or pre-treatment in the same growth run.

Assessment of the effectiveness of surface cleaning treatments is difficult in a system which does not have any in-situ surface physics. After cleaning, substrates have to be removed from the MOVPE system for assessment. This results in immediate contamination of the surface with oxygen and carbon on exposure to the atmosphere.

In quarter 11, we reported that silicon substrates can be prepared in a UHV system, encapsulated in metallic arsenic, then taken out in to the atmosphere prior to growth in an atmospheric pressure MOVPE system. It was not possible to carry out the reverse procedure because the amorphous arsenic deposited from the MOVPE process did not protect the silicon surface from contamination.

The only assessment that could be readily applied was to deposit GaAs under a standard set of conditions, and assess the effectiveness of the substrate cleaning by the quality of the epitaxial growth.

The standard conditions were as follows:

The standard cleaning procedure was to heat the substrate with its native oxide in hydrogen at 950^{0}C for 30 minutes. A GaAs/AlAs superlattice was grown at 400^{0}C and annealed for 20 minutes at 750^{0}C. All subsequent layers were grown at temperatures between 720^{0}C and 750^{0}C. This procedure gave uniform epitaxial layers up to 3μm thick, with X-ray diffraction (004) reflection full width half maxima, FWHM, of typically 250 arc seconds and a specular surface free from microscopic pits.

Variations on the standard conditions included:

(i) Chemical pre-treatment

Etching of the silicon to remove the native oxide and replace it with a thinner, more easily evaporated, layer was carried out using the "RCA" and "Shiraki" etches. Simple dipping in concentrated hydrofluoric acid was also used. None of these procedures improved the substrate cleaning. Auger

electron spectroscopy showed that the surface of the silicon could be stabilised against rapid oxidation by immersion in buffered hydrofluoric acid for 20 minutes. This treatment did not result in improved epitaxy. The standard condition chosen was therefore to employ the wafers with their as-received native oxide.

(ii) Atmospheric composition

Because the cleaning of silicon depends on the reduction of silicon dioxide to monoxide, followed by evaporation of the monoxide layer, anything that might result in a more reducing atmosphere would be expected to improve the cleaning. The principal reducing agent is atomic hydrogen, it follows that an increased concentration of this should result in better cleaning. The inclusion of arsine or silane in the cleaning gases should therefore be expected to give improved cleaning due to the decomposition of the arsine to arsenic and hydrogen, or the silane to silicon and hydrogen. Silicon produced by the heterogeneous decomposition of silane will also reduce SiO_2 to SiO, enhancing the cleaning process. Substrate cleaning in AsH_3/H_2 mixtures and SiH_4/H_2 mixtures was investigated. No improvement over the standard hydrogen clean was observed.

(iii) Pressure

Reducing the partial pressure of oxygen and water vapour in the reactor can either improve the substrate cleaning or enable a reduction in the cleaning temperature, in accordance with the data of Ghidini and Smith and that of Lander and Morrison. The system base pressure capability was 10^{-3} Torr and oxygen/water vapour partial pressures were estimated to be in the region of 2×10^{-4} torr. The predicted minimum temperature for thermal cleaning to be effective under these conditions is 930^0C, and this agrees well with our observed minimum successful thermal cleaning temperature of 937^0C.

(iv) Temperature

950°C represented the maximum that could be achieved with the low pressure apparatus employed for this study. Reduction of the temperature might be

considered feasible along with a variation of the other conditions, but it was not found possible to reduce the cleaning temperature under any of the conditions and retain reasonable epitaxy, due to the partial pressure limitations discussed in (iii).

(v) Orientation

The standard substrate orientation used, 3^0 toward (010), was that reported as giving freedom from antiphase domains in MBE epitaxy. Misorientated (100) substrates tilted 3^0 towards [110], and on-orientation (100) substrates within ± 0.5 degrees, were also used. No difference was found in morphology or full width half maximum measurements for the misoriented substrates, however, a greater defect density and poorer uniformity were found for the on-orientation substrates. The best full width half maximum of 170 arc secs was obtained using an on-orientation substrate.

(vi) Time

Prolonged cleaning times, greater than the standard 30 minutes, showed no improvement.

(vii) Plasma

An in-situ microwave plasma will result in a greater concentration of atomic hydrogen. Because of the configuration of the MOVPE apparatus the microwave plasma had to be generated remotely from the substrate and the concentration of atomic hydrogen was thus reduced by recombination after generation at the microwave cavity. A disadvantage of this method was that the atomic hydrogen reduced the fused quartz at the cavity which could result in contamination of the substrates with silicon oxide. Nevertheless, excellent full width half maximum results could be obtained by this method, although the result proved difficult to reproduce. The use of a plasma necessitated operation at pressures of less than 20 torr. This had the disadvantage that at these lower pressures, the effective partial pressure of the residual contaminants, water vapour, oxygen and carbon, are raised in comparison to growth at atmospheric pressure. A possible explanation for the disappointing plasma

results could be due to the plasma forming a more reactive oxygen species from residual oxygen and moisture, thereby giving a strongly competing oxidation reaction.

(vii) Selected area epitaxy

Trial growth runs under the standard conditions were carried out using on-orientation silicon nitride masked substrates. A FWHM result of 193 arc seconds was obtained for the SAE sample compared with that of 265 arc secs for a conventional misoriented specimen processed at the same time. The masked substrate, however, showed a higher incidence of surface defects.

Directly after the growth of GaAs onto a silicon IC, it will be necessary to remove polycrystalline GaAs from Si_3N_4 or SiO_2 areas so that the silicon transistors below can be revealed and processing continued. Chemical etching experiments upon the wafers grown on this programme showed the polycrystalline GaAs to be very difficult to remove.

It follows that, for the establishment of a silicon IC process incorporating GaAs circuits, a form of ion beam etching will be required to remove this polycrystalline GaAs. This should not present a problem as reactive ion etching (RIE) is now an integral part of all silicon processes.

Growth at lower pressures may enhance the selectivity of the growth, thus leading to total selectivity, eliminating the need for any ion etching of the GaAs.

2.1.3 Assessment

2.1.3.1 Optical Microscopy

Surface defects were examined using interference contrast microscopy. The presence of pits was taken as an indication that the surface cleaning procedure had not been successful and the subsequent layer growth was either polycrystalline or the initialisation layer was discontinuous leading to 3-dimensional growth and surface roughening.

2.1.3.2 X-Ray Diffraction

The full width half maximum of the (004) X-ray diffraction reflection was also measured.

It was found that the FWHM measurements did not generally reveal a good correlation with the defect density determined by interference microscopy.

2.1.3.3 Transmission Electron Microscopy

Transmission electron microscopy was carried out on those layers in which growth had taken place successfully, ie, visually specular surface, low defect density by optical microscopy, and X-ray diffraction FWHM less than 300 arc sec. No evidence of anti-phase domains was found and no difference was observed, between the behaviour of (100) substrates misoriented towards the [011] and towards [110] directions.

The best layers contained $\sim 1 \times 10^8 cm^{-2}$ TD, as measured by plan-view TEM. This result is good considering that no SLS dislocation filters can be included in layers grown on the low pressure experimental reactors used.

2.2 COMBINATION OF CTA, SLS, AND PROFILED SUBSTRATES

The materials effort during this quarter has been directed to the successful deposition of epitaxial gallium arsenide on silicon using a combination of cyclic thermal annealing (CTA), incorporation of GaInAs/GaAs SLS, and profiled substrates, for the same growth run.

In quarter 11 we reported initial experiments in which there had been problems in controlling the GaInAs/GaAs SLS. It was also established that the selectivity of deposition between the free surface and the "V" groove channel was reduced for growth at atmospheric pressure. This resulted in some infilling of the "V" groove channel, but toward the top of the groove, with a well defined (111) facet, see Figure 2.2.1.

A further series of substrates were prepared as described in Q11 pages 10 and 11. After loading into the atmospheric pressure reactor, and flushing

with hydrogen, the silicon was thermally cleaned at 1100°C for 4 mins prior to the low temperature initial growth at 400°C, and anneal at 850°C, i.e. the first stage of the usual 2-step growth process. 200Å of GaAlAs were then deposited at 650°C followed by a thermal anneal for 20 mins at 850°C and then cooling to 400°C before returning to the growth temperature which was 650°C. This cycle was repeated five times. 2.16μm of GaAs was then grown followed by two bands of 10 periods of $Ga_{0.85}In_{0.15}As$/GaAs SLS separated by a 300Å spacer. The total layer thickness of this structure, see fig.2.2.2, was 4.2μm. Optical microscopy showed conformal growth over the wafer with the usual GaAs/Si surface morphology, and a thinning of the deposit in the "V" groove channels. X-ray diffraction peak widths FWHM of 150-200 arc secs were obtained for this material.

Transmission electron microscopy, TEM, of this specimen is reported below.

3. TEM STUDIES

3.1 INTRODUCTION

The removal of threading dislocations from active device areas has been highlighted as one of the principal objectives behind achieving device quality GaAs grown onto a silicon substrate. One of the proposed methods by which significant reductions in threading dislocations can be achieved is by the patterning of substrates so that dislocations, gliding under a mismatch stress, can be lost to a patterned feature edge. In Quarter 11 TEM was reported upon GaAs deposited onto patterned dielectric and mesa substrates. Also reported was the optical microscopy of V-grooved substrates suitable for the growth of GaAs on Si. For this quarter we have studied the microstructure of GaAs deposited onto the V-Grooved Substrates. In this section we shall present the analytical TEM results. A full discussion, contrasting the methods by which material may be improved, is included in the final summary, section 4.4, of this report.

3.2 EXPERIMENTAL

The V-grooved substrate was prepared as shown in the quarter 11 report. It was prebaked at 1100°C for 4 minutes under H_2 and then the GaAs structure shown in Figure 2.2.2 was grown. This has been studied by both [110] cross-section and [001] planar view TEM to assess material quality.

3.3 RESULTS AND AND DISCUSSION

Figure 2.2.1 shows an SEM micrograph of a V-groove between two mesa areas. The ~4μm of epitaxial GaAs is clearly visible on the top of the mesa's. It thins to approximately 0.4μm at the side of the groove. The [110] TEM cross-section of figure 3.3.1 shows that the material grown on the {111} sidewalls of the V contains many planar defects (stacking faults and microtwins) and contains misoriented grains. This highly defective region does not extend above the level of the mesa top, giving us single crystal {111} upper sidewalls. Once the GaAs has conformally coated the silicon substrate, and this has been annealled, we assume that misfit dislocations will be formed in this heterointerface as discussed in the quarter 10 report. GaAs, as expected, shows a slower growth rate for the denser packed and lower surface energy {111} plane rather than the {001}. This is the principal reason for the deposit on the sidewall being much thinner. The relative thicknesses suggest a 10:1 ratio for {001}:{111} growth rates. These values will also take into consideration any changes in growth rate due to possible reagent depletion in the V groove during MOVPE growth. The high density of planar defects upon the sidewall is not a surprise if we follow the arguments that are outlined in the quarter 11 report for the formation of microtwins and stacking faults on exposed growing island edges. It is easy for the adatoms constructing the nuclei on a {111} face to translate to adjacent sites forming a stacking fault in the interface plane and between this nucleus and other coalescing nuclei. The principal behind this was first outlined by Booker and Stickler[1]. It is more recently discussed by Pirouz[2]. Because of the slower growth rate on the {111} plane the initial layer would have been thinner than 200Å and most probably semi-continuous. For {001} epitaxy a continuous pre-layer, that is pre-baked to remove planar defects

and enable regular misfit dislocation arrays to form, has been shown to be essential for good epitaxy. If the {111} sidewall growth is not continuous then the conditions for good epitaxy will not have been met. This, coupled with the higher misfit dislocations interfacial energy on the {111} plane, is the probable explanation for the appearance of planar defects and misoriented grains on this sidewall. The upper part of the sidewall is good single crystal. It is this part of the structure that is important for defect filtering, the single crystal allowing sufficiently motivated dislocations to glide to the free surface unhindered.

Figure 3.3.2 shows a montage of a 39μm wide mesa. The two strained layer superlattice dislocation filters can be seen toward the centre of the layers. To work efficiently the dislocation filters have to be able to move the threading dislocation segments to a free surface. Closer inspection of the sidewall (fig. 3.3.3) shows the dislocation filters at the sidewall edge. The dislocation filter does not terminate at the edge because the {111} plane continues to grow for all layers subsequent to the first strained layer. The result is 0.23μm of GaAs sidewall growth over the strained layer edges for a subsequent deposition of 1.25μm of GaAs after the SLS growth. The micrograph shows dislocations terminating at the free surface, these are labelled D. This shows the effectiveness of this sidewall as a dislocation sink. The structure at this sidewall is created as follows; after the deposition of several of the strained superlattice periods the strain is sufficient to force the threading dislocation portion in the strained layer superlattice (SLS) to migrate away from that below the SLS forming the lengths of misfit dislocations that are seen in the strained layer filter to GaAs interface. If the migration length is sufficiently long and/or the sidewall edge is sufficiently close then the threading segment in the epilayer will be lost to this surface, thus reducing the threading dislocation density. This is shown schematically in fig.3.3.4(a). As further epilayers are grown onto this structure then growth also occurs on the {111} sidewalls which will extend the terminating threading dislocation portion to form the structure shown in fig.3.3.3. This is represented in fig.3.3.4(b).

Plan view TEM analysis from these small (39μm x 15μm) areas is very difficult due to problems with sample preparation. It is, however, possible to analyse

long stripes (200μm x 15μm) from the same material. Analysis of these stripes showed them to contain 1.6 x 10^7 cm^{-2} threading dislocations. These long stripes can be shown not to be representative of the defect densities in the smaller areas. Dislocations glide in [110] or [$\bar{1}$10] directions (for [001] epitaxy). The average dislocation glide length that is observed is between 10 and 20μm. For the 15μm x 39μm mesa threading dislocations that glide parallel to the 15μm mesa side should all be lost to the free surface. For dislocations gliding parallel to the 39μm side most will still be lost ie an area of between ~10 and 20μm wide should be depleted along the mesa edges. For the structure that was studied by plan view TEM, dislocations that are parallel to the long (200μm) sides will, in the most part, not be able to be lost because their glide length is too short. Similar structures, to this wafer grown onto planar substrates, exhibit threading dislocation density N_D, of between $7x10^7 cm^{-2}$ and $1.5x10^8 cm^{-2}$. For our stripe we would thus expect, a total loss of dislocations in its short dimension and little change in its long dimension. The threading dislocation density remaining will hence be $\sim 0.5N_D$ i.e. $3.5 \rightarrow 7.5x10^7 cm^{-2}$. Our observed value of $1.6x10^7 cm^{-2}$ thus appears very promising when compared to these figures.

3.4. CONCLUSIONS

Threading Dislocations are lost to the mesa edges. This has been shown to be an effective method by which residual defect densities can be reduced. This topic is discussed in the final summary (attached to the end of this document) where new ideas are presented that can gain maximum benefit from these dislocation sinks.

4. END OF PROJECT REVIEW - SUMMARY OF PROGRESS

4.1 SUBSTRATE PREPARATION AND CLEANING

It was found that silicon substrate surfaces could not be cleaned satisfactorily at temperatures less than 940°C in the low pressure MOVPE system using a hydrogen carrier gas at 100 Torr. This limitation was believed to be due to the partial pressure of residual moisture and oxygen in the MOVPE system.

Although R.F. and microwave plasmas were employed to increase the concentration of reactive hydrogen, the configuration of the apparatus did not enable efficient generation of an active hydrogen species in a sufficiently close proximity to the substrate surface. This prevented any significant reduction in cleaning temperature to be obtained using plasmas because no effective bombardment took place between the plasma and the substrates.

A significant improvement could be obtained by redesigning the apparatus to reduce the separation between the plasma and the substrates. This would ensure a greater concentration of active hydrogen in the substrate region, and would also permit controlled ionic bombardment of the substrate.

4.2 SUBSTRATE ORIENTATION

In the atmospheric pressure system, epitaxial growth of GaAs on silicon was carried out using our normal 2-step growth routine preceeded by a high temperature substrate thermal clean at ~1150°C. The most successful results were obtained using on orientation substrates (100)±0.5°. Specular surfaces were obtained routinely, double crystal X-ray peak widths, FWHM, were between 150-300 arc seconds, and antiphase domains were not observed. Investigations of deposition of GaAs on silicon substrates orientated (110), (111), (211) and (100) tilted 2° and 4° towards the nearest [110], and tilted 3° towards [111], were carried out using a "standard" (100) wafer as a control specimen. In each case surface morphologies were inferior to those obtained on the control specimen. The (100) tilted toward [111] specimen contained lower residual doping than the control specimen. This was reported in detail in quarterly report No.9 Sept-Nov. 1988.

In the low pressure MOVPE system used for surface cleaning experiments, specular surfaces were more often obtained, after appropriate adjustment of the initial nucleation conditions, when off orientation {100} substrates were used.

The use of off-orientation substrates is reported to result in a reduction in type II misfit dislocations and to more readily generate silicon surfaces

consisting predominately of diatomic steps, a reported essential requirement for minimising Antiphase Domain (ADP) formation. For on orientation wafers, the high temperature prebake also results in a diatomically stepped surface.

These observations show that in addition to obtaining an atomically clean surface, surface reconstruction and layer nucleation play a key role in obtaining epitaxial layers with low APD, and low residual doping.

4.3 OPTICAL MICROSCOPY & DEFECT ETCHING OF GaAs ON Si

The use of conventional Nomarski interference contrast optical microscopy for the examination of epitaxial layers of GaAs on silicon substrates has a number of advantages over other techniques such as scanning electron microscopy (SEM) and transmission electron microscopy (TEM). Apart from ease of use, speed of examination and relative cheapness of the equipment required, the principle advantage is that large areas can be examined, so that clustering of defects, for example at a localised damage region of the substrate, can be quickly and easily spotted. Another unique strength of the technique is that it is non-destructive so that exactly the same area can be studied after repeated treatments, so that a type of depth profiling can be achieved. This approach was found to be particularly useful in the examination of defects revealed by etching. However, before these various advantages of the optical technique can be exploited it is essential to undertake careful calibration experiments using additional methods, such as TEM, in order to establish the validity of the experimental observations. In addition, there are clear limitations imposed by the use of an optical microscope with its considerably reduced resolution compared with TEM or SEM. Another limitation is that values, such as the Burgers vector of a dislocation, cannot be determined using optical microscopy.

A considerable amount of information was obtained by examination of as-grown GaAs layers on Si, although the interpretation of the observed features often required additional treatments and the use of additional examination techniques. Briefly, the as-grown layers show surface topology which can be related to the orientation of the substrate, stacking fault features, and fine linear markings predominantly in one <110> only (for epitaxial layers

> approximately 4μm thick) which are cracks resulting from the thermal mismatch between layer and substrate. The use, for the first time, of a well-known silicon etch (the Wright etch) as a GaAs etchant enabled dislocations in the epitaxial layers to be examined, through the production of etch pits where the dislocations intersected the epitaxial surfaces. Unlike several other etchants which had previously been reported to give erroneous etch pit counts when compared with TEM dislocation density estimates it was found that excellent agreement between etch pit positions and TEM observed line dislocations could be achieved, by using TEM examinations of Wright etched epitaxial layers. It was concluded that etch pit density values would "saturate" at $\sim 5 \times 10^7 cm^{-2}$ for TEM dislocation densities $> 5 \times 10^7 cm^{-2}$, because the inherently lower resolution of the optical microscope limits the visibility of etch pits which are required to be kept small (~0.5μm diam.) in order to avoid counting errors due to overlapping pits. For dislocation densities $< 5 \times 10^7 cm^{-2}$ the agreement between optical and TEM values could lie within a factor of 2 or 3.

The use of the Wright etchant also enabled interesting observations of stacking fault partial dislocations, and cross-hatch pattern distributions within epitaxial layers to be made. In addition, by combining this method with low temperature (10K) cathodoluminescence wavelength shifts it was possible to demonstrate on a microscopic scale, how the in-plane biaxial tensile stresses in the thicker epitaxial layers was relieved, within ~30μm distance of the <110> thermal mismatch cracks.

4.4 DEFECT REDUCTION

Considerable effort has been made to reduce the crystallographic defect densities of the GaAs epilayers. Defect reduction has been achieved in two areas. Planar defects (i.e. stacking faults and microtwins) have been reduced by the use of a low temperature, thin, semi-amorphous layer of a GaAs/AlAs superlattice to initiate growth followed by a high temperature anneal. Prior to annealing, this layer contains $\sim 1 \times 10^{11} cm^{-2}$ planar defects, however, after annealing this drops to $< 1 \times 10^{10} cm^{-2}$ and subsequently falls to $< 10^5 cm^{-2}$ with continued high temperature growth. This procedure is very

efficient at reducing the planar defect densities to relatively insignificant levels. The anneal procedure also homogenises the strain distribution within the layer, introducing regular misfit dislocation arrays into this heterointerface. Any local rotation is removed from the layer which ensures that it becomes an excellent 'substrate' for further growth of GaAs.

These layers of GaAs contain a large number of threading dislocations (TD), these being an unavoidable and undesirable by-product of the misfit dislocations formed at the heterointerface. TD densities have been measured by Plan-view TEM. Within the density regime studied, this technique provides the most accurate figures. There are $\sim 1 \times 10^{11} cm^{-2}$ TD generated from the GaAs:Si heterointerface. Strained layer dislocation filters have been used to reduce the TD density. These have principally been Strained Layer Superlattices (SLS). During these studies it has become apparent that for efficient dislocation filters it is necessary, not only to choose the correct SLS configuration, but also to grow sufficiently thick spacers between the SLS. Experimentally determined guidelines, developed during this program, have enabled TD densities to be reduced from 10^{11} to $10^{7} cm^{-2}$ in only 3.5μm of epilayer. If it were possible to continue growing and filtering to larger thicknesses then it would, of course, be possible to reduce this density to improved values. This has been shown recently by Tachikawa et al[1] who grew a layer to 180μm thickness to achieve $10^{5} cm^{-2}$ TD. The thermal expansion mismatch between the GaAs and the Si, however, restricts the useful thickness of this epilayer. The lattice mismatch incurred by cool down, coupled with large layer thicknesses, generates a large tensile shear stress at the heterointerface forcing the epilayers to crack. Our experiments show that for layers over $\sim 3\mu m$ thick the cracking becomes significant rendering the wafer unsuitable for device fabrication.

The dislocation densities that have so far been achieved are sufficiently low for FET and Detector applications, as has been demonstrated by this project. The performance of these devices can be expected to improve, and perhaps for other devices such as emitters their operation enabled, by further reductions in TD density. To achieve this we have applied selective area epitaxy to the growth of GaAs on Si. This is detailed in section 4.6.

4.5 GROWTH OF OTHER III-Vs ON SILICON

GaInAs layers on silicon have been used in superlattice structures designed to operate as dislocation filters. In a separately funded project, we have also grown and fabricated GaInAs detectors on silicon substrates.

Recently we have also attempted to grow InP on silicon using a low pressure MOVPE system dedicated to InP based materials growth. Access to this MOVPE system was limited due to the heavy commitment to the InP based materials growth program, hence, only a limited series of experiments could be carried out. In the course of these experiments it became obvious that we would need a much longer period of experimentation before InP could be grown on silicon in a controlled and reproducible manner.

The initial experiments produced material in which the InP layer nucleation was three dimensional this being linked to a problem with in-situ substrate cleaning where the maximum temperature available was ~850°C.

It was felt that in the brief time remaining on this program, a prolonged investigation of substrate cleaning and layer nucleation in this particular MOVPE system could not be carried out.

4.6 SELECTIVE AREA EPITAXY (SAE)

Selective area epitaxy shows two distinct advantages for the growth of GaAs on silicon. SAE can provide enhanced dislocation filtering. It also can be used for deposition into discrete areas on a silicon VLSI wafer, from which devices can be formed.

A SLS filter forces a threading dislocation (TD) to glide sideways. If a TD can reach the edge of the wafer then it can be lost to this edge. The use of SAE brings an edge closer to the moving TD thus more are lost to it, and the residual TD density is reduced. If SAE is performed into windows cut into an oxide formed onto a silicon VSLI wafer then areas of GaAs devices can be fabricated into the silicon circuit which should display lower TD densities.

Deposition onto a patterned oxide wafer indicated that contamination of the windows from the oxide area may occur prior to epitaxy, however the use of patterned substrates has been proven to reduce TD densities. TD have been observed to be lost to sidewalls generated by SAE, proving that it is a viable method by which TD densities can be reduced. Improved detectors have been demonstrated by this method [3].

4.7 OPTO-ELECTRONIC DEVICES IN GaAs ON SILICON

Early in the program both GaAlAs/GaAs LEDs and QW lasers on silicon were investigated. These devices had limited life-times due to rapid degradation associated with the high density of threading dislocations which penetrated the active layer, typically $\sim 10^7 cm^{-2}$. Ideally the defect density has to be reduced to $< 10^3 cm^{-2}$ before efficient, long lived C.W. emitters can be fabricated. For this reason we decided to concentrate our effort on materials improvement, and not attempt fabrication of light emitting devices until significant materials improvement had been achieved.

4.8 ELECTRONIC DEVICES

GaAs on silicon MESFETs were fabricated in GaAs on silicon. D.C. parameters equivalent to homoepitaxial devices were obtained but R.F. performance was compromised due to substrate conduction. Undoped $Ga_{0.4}Al_{.6}As$ buffer layers were used in these devices. It was difficult to achieve high resistance GaAs on Silicon. Homoepitaxial GaAs grown at 650°C at low V:III ratios of between 5:1 to 8:1 had carrier concentrations $< 10^{14} cm^{-3}$ and 77K mobilities in the range 80,000 - 100,000 $cm^2 V^{-1} S^{-1}$. Identical growth on silicon resulted in materials with $N=10^{15} cm^{-3}$ (best value) to $N=10^{16} cm^{-3}$, and 77K mobilities in the range 20 - 30,000$cm^2 v^{-1} s^{-1}$. Transition metal doping Cr,V, resulted in high resistance material with sheet resistivities $> 10^8$ ohms/sq, but these dopants tended to either diffuse into the FET structure or contaminate the MOVPE reactor.

Heterojunction bipolar structures on 3" wafers were also grown. These devices showed low gains ~ 1. The low gains are principally atributed to non-

optimised doping conditions. There may also be a degradation of performance via non-radiative recombination by the high dislocation density.

4.9 OPTOELECTRONIC INTEGRATION

The main incentive for research into the growth of III-Vs on silicon substrates has been the possibility of integrating advanced silicon microelectronic I.C.s with optoelectronic III-V devices on a single wafer without having to resort to bonding techniques, such as flip chip bonding etc. At the end of this project it is apparent that the implementation of full silicon - III/V integration is limited by the following constraints:

(i) Thermal expansion misfit - resulting in wafer bowing and layer cracking.

(ii) High densities of threading dislocations $\sim 10^7 cm^{-2}$ which prevent successful CW operation of light emitting devices such as lasers and LEDs.

(iii) A high temperature thermal clean of the silicon substrate surface which will damage existing processed or part processed silicon wafers.

(iv) Difficulty in obtaining clean surfaces in the mask window areas for selective area epitaxy.

In spite of these constraints the incentive for optoelectronic integration remains strong, and a technical breakthrough would have enormous advantages. For a project continuation our recommended approach is as follows:

(1) Set up a more extensive and vigorous investigation of low temperature substrate cleaning, using a microwave plasma source, and surface physics to monitor surface cleaning and conditioning.

(2) Carry out further investigations of selective area epitaxy using low temperature surface cleaning and MOVPE growth at low pressures in the range 1-50 Torr.

(3) Investigate very thin ~1μm dislocation filters based on GaInAs/GaAs or GaAsP/GaAs SLS with the objective of making these structures dual function e.g. combined dislocation filter and photodetector or reflector layers.

(4) Develop improved dislocation filtering by thermal activation of dislocations at SLS defect filters.

(5) Investigate growth and fabrication of III/V on silicon quantum confirmed. Stark effect optical reflection modulators and photo-detectors.

(6) Integrate these structures with silicon CMOS wafers using SAE.

The result of this R & D would yield a route to CMOS compatible on chip optical receivers and reflection modulation transmitter terminals for low power, high performance optical interconnection of VLSI.

5. CONCLUSIONS

5.1 DEFECT REDUCTION

5.1.1. Removal of planar defects

An efficient method of removing planar defects from the epitaxial layers of GaAs on Si has been achieved. These can be reduced to $<10^5 cm^{-2}$ which is lower level of detection by TEM.

5.1.2. Removal of threading dislocations

(i) Threading dislocations can be removed by the use of SLS dislocation filters. The use of thick spacers >1000Å between the SLS filters is necessary to achieve efficient dislocation reduction.

(ii) The base level achievable, prior to the onset of layer cracking from thermal expansion mismatch, by the use of strained layer filters and spacer combinations is $1x10^7 cm^{-2}$.

(iii) This figure can be lowered by the adoption of selective area epitaxy. Threading dislocations have been observed to be lost to the edges of the selected areas, reducing their density into the range 10^6-$10^7 cm^{-2}$ or below.

(iv) The adoption of selected area epitaxy and further experimentation to enhance dislocation mobility by thermal activation, should enable the reduction of threading dislocations to much lower levels than have been reported in this project, or have been substantiated in current literature.

5.2 THERMAL EXPANSION

The almost 3 fold difference in thermal expansion coefficients between GaAs and Si is a fundamental problem limiting the GaAs layer thickness to approximately 3μm prior to cracking. If thicker layers could be grown without cracking, for example, by using selective area epitaxy defect densities could be reduced dramatically.

5.3 SUBSTRATE CLEANING

Although reproducible GaAs on Si epitaxy can be demonstrated successfully on silicon substrates which are thermally cleaned at temperatures in excess of 1,100°C, an equally reliable low temperature, <900°C, silicon cleaning process has yet to be demonstrated before processed silicon wafers can be used for GaAs epitaxy. The low temperature cleaning experiments carried out during this project suggest that plasma cleaning techniques could be futher advanced to enable substrate cleaning at temperatures <900°C.

5.4 LAYER NUCLEATION

The 2-stage growth process, in which an initial 300Å layer is grown at 400-450°C, and is then subsequently annealed at 850°C, followed by epitaxial

growth at 650-720°C has proven to be the most successful route for epitaxial III-Vs in silicon.

5.5 ANTIPHASE DOMAINS APD

Antisite disorder was not usually observed by conventional or convergent beam TEM, in epitaxial GaAs/GaAlAs grown on (100) orientated silicon substrates using the 2-stage growth process, from which it is concluded that either APDs are totally absent, or there is a large separation between them.

5.6 SUBSTRATE ORIENTATION

On orientation (100) silicon substrates thermally cleaned at >1100°C in hydrogen produced the best quality epitaxy in the atmospheric pressure MOVPE system. For growth at reduced pressure 10-100 Torr, and for wafers cleaned at ~950°C, (100) substrates tilted towards [111] gave the best morphology and X-ray diffraction FWHM = 170 arc secs.

5.7 OTHER III-V ON SILICON

Growth of InP and InP related alloys on silicon requires further development of the initial nucleation and anneal stages of the 2-step growth process.

5.8 OPTO ELECTRONIC DEVICES

Emitters fabricated in GaAs on silicon have low electroluminescent efficiencies and the devices are short lived.

GaInAs on silicon photodetectors with leakage current densities of 1.3 x $10^{-4}Acm^{-2}$ at -5V bias and external uncoated quantum efficiencies of 59% at 1.3μm.

5.9 ELECTRONIC DEVICES

HBTs, being minority carrier devices, could have their device performance compromised by the high defect densities. HBTs with gains of ~1 were

obtained in GaAs on silicon, however, this performance may be improved by further optimisation of the device doping characteristics.
FETs being majority carrier devices are not seriously affected by the high defect density and these devices fabricated in GaAs on Silicon had characteristics comparable with homoepitaxy devices, e.g. transconductances of $180mSmm^{-1}$ for $\sim 0.7\mu m$ gate width were obtained for GaAs/Si FETs.

6. RECOMMENDATIONS

THE POTENTIAL FOR OPTO-ELECTRONIC INTEGRATION

This programme has tackled the principal problems behind growing GaAs on Si. Thermal expansion mismatch (and hence cracking), planar defect formation, island nucleation (and thus poor morphology), anti-phase domain formation and threading dislocation removal have all been considered. At the termination of the practical side of this programme Plessey Research had developed a growth procedure that had narrowed all of these problems to the control of one parameter, that of residual threading dislocation density.

Residual threading dislocation density has been reduced dramatically by the use of various strained layer filter and spacer combinations. The threading dislocation densities have also been demonstrated to be reduced by the use of selected area epitaxy where they have been observed to terminate at the area edges. The residual threading densities do not prevent operation of detector or FET structures. If we wish to improve this material quality and the device performance then we must adopt a research strategy that will concentrate upon selective area epitaxy and enhancing the mobility of the laterally gliding threading dislocation at the SLS filter. We have already established a firm basis for this research, proving the effectiveness of selected area edges as dislocation sinks and indicating that the threading dislocation density can be reduced to less than has so far been achieved.

It remains for us to speculate upon how the applications for such material have changed over the 3 year duration of this programme and how research strategies, if implemented, could provide a material of desired specification

for a useful application. GaAs on Si FETs are poorer in RF performance than both silicon MOSFETs and GaAs MESFETs. At the present time there is no specific advantage in using GaAs on Si MESFETs. GaAs detectors, which have already been successfully demonstrated, would have a major use if they can be made to work in conjunction with optical modulators. Modulator and detector elements embedded into a VLSI CMOS circuit would render silicon IC optoelectronic communication feasible by bonding the IC onto an optoelectronic mother board patterned with waveguides.

Other IC's would also be bonded to this circuit such that the waveguides interconnect the modulator and detector elements on all chips. This circuit is then driven by a laser chip also bonded onto the OEMB.

This application of optoelectronic interconnection for silicon IC's makes the growth of GaAs onto a Si VLSI circuit very desirable. The knowledge and understanding that has been gained from this project has brought this long term milestone much closer to reality.

7. REFERENCES

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2. Pirouz P, Ernst F and Cheng T T (1988) Mat. Res. Soc. Proc. Vol. 116, 57.

3. Hodson P D, Kightley P, Goodfellow R C, Joyce T B, Riffatt J R, Bradley R R and Griffiths R J M, Semicond. Sci. Technol. (1988), 3, 715.

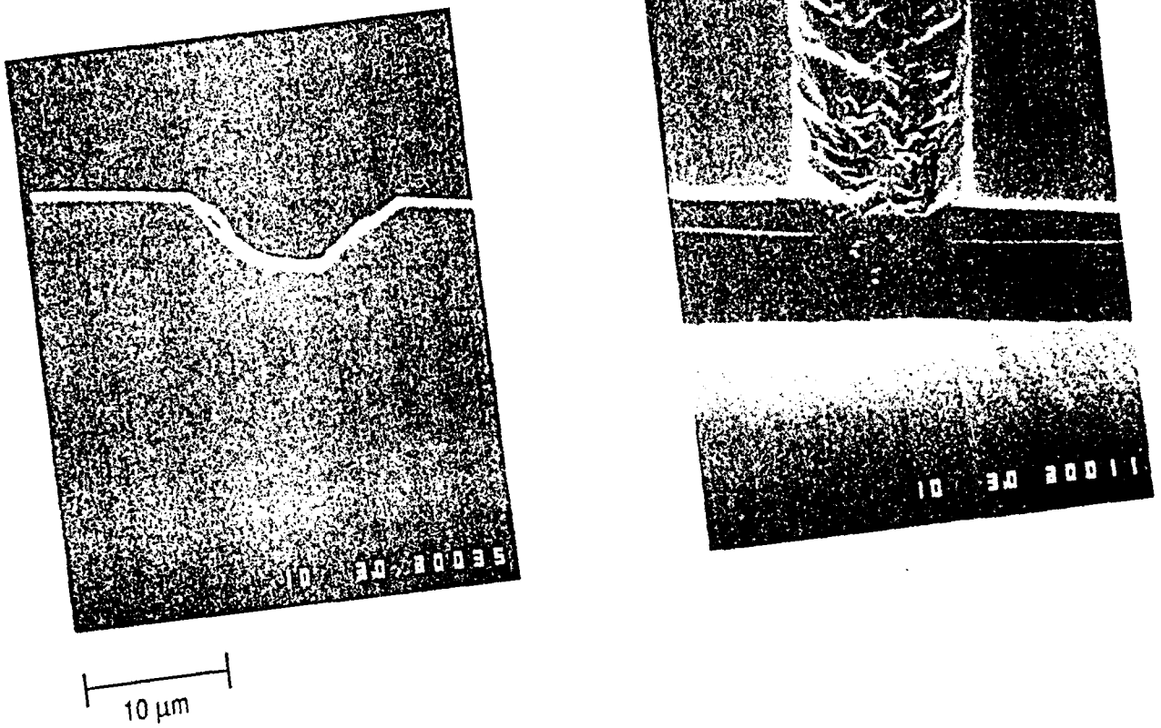
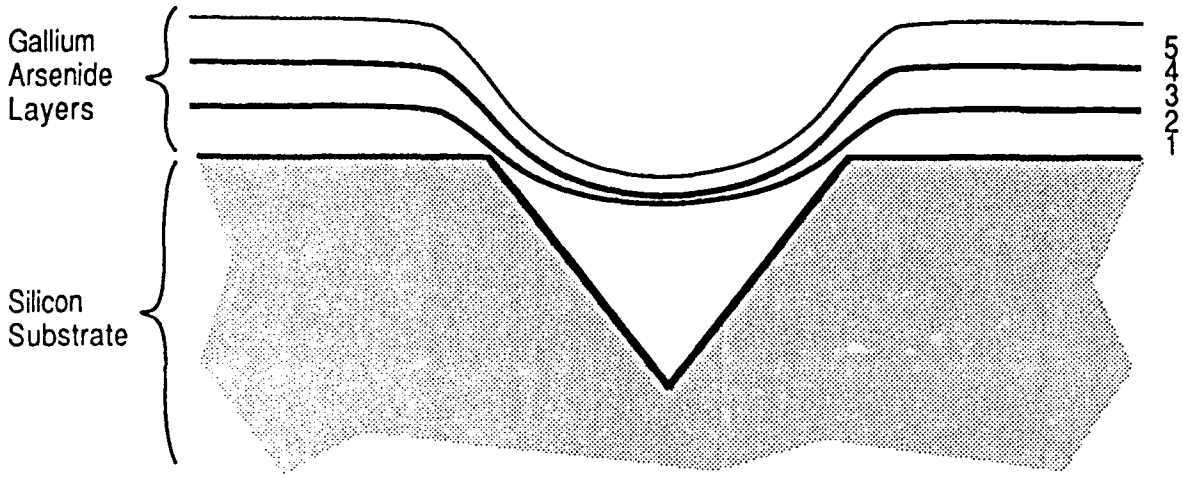


Fig 2.2.1 S.E.M. OF GaAs GROWTH IN 'V' GROOVE



LAYER STRUCTURE

Layer 1 - GaAs 2.16μm
Layer 2 - GaInAs/GaAs SLS 0.25μm
Layer 3 - GaAs 0.30μm
Layer 4 - GaInAs/GaAs SLS 0.25μm
Layer 5 - GaAs 1.24μm

Each SLS contains 10 periods of $Ga_{0.85}$ $In_{0.15}As/GaAs$

Fig 2.2.2 GaAs ON SILICON USING 'V' GROOVED SUBSTRATES, CYCLIC THERMAL ANNEALING AND SLS

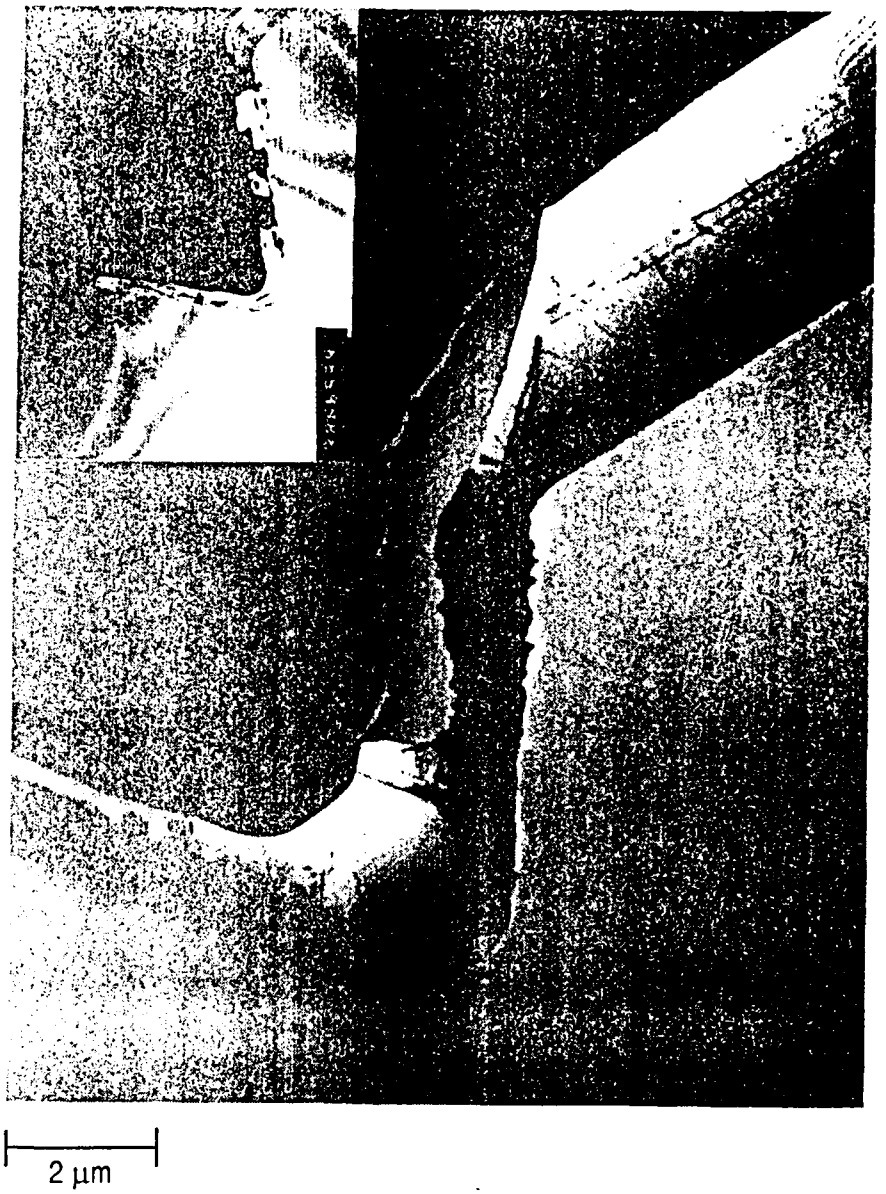


Fig 3.3.1 CROSS-SECTION TEM SHOWING THE SIDEWALL STRUCTURE

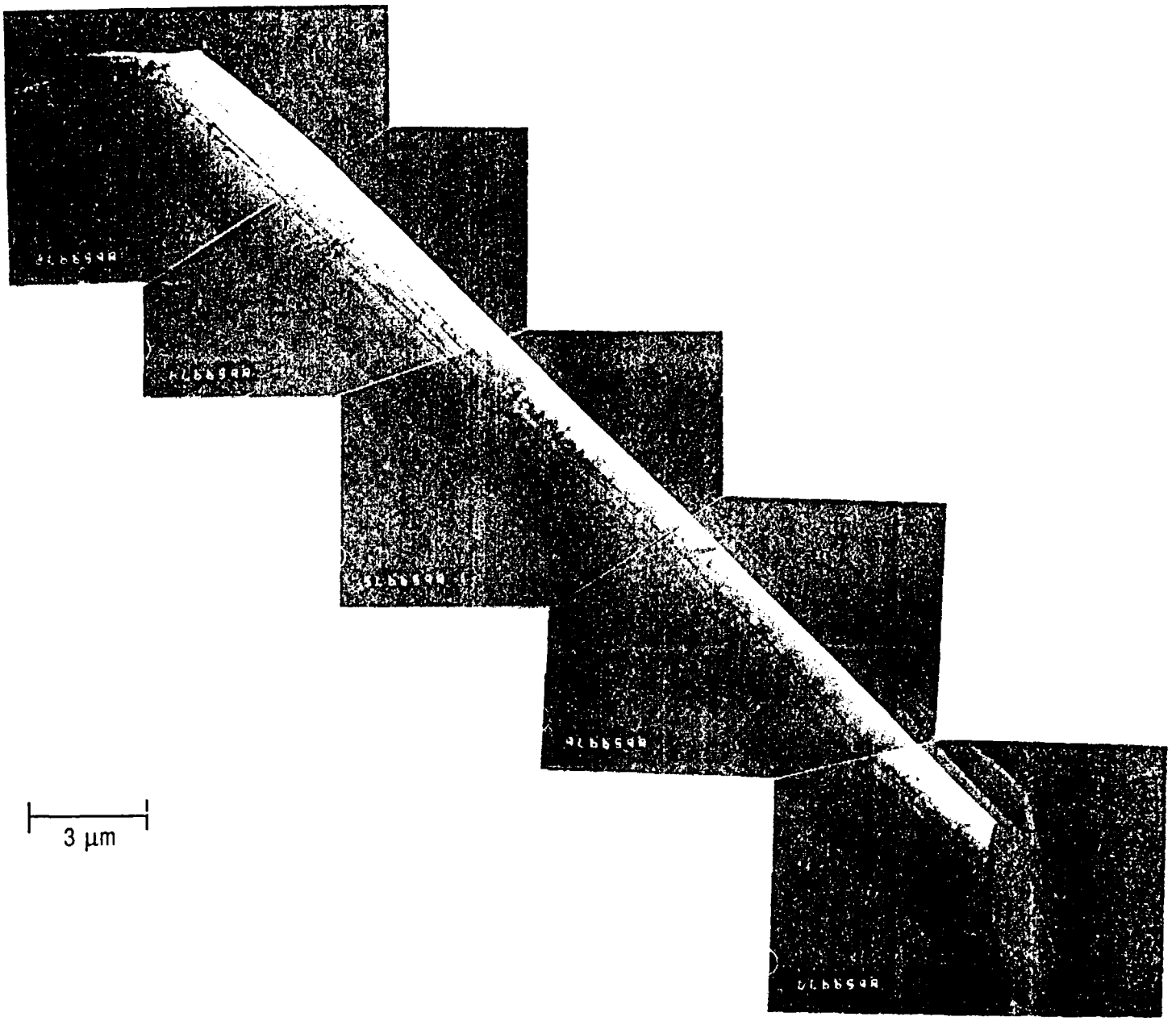


Fig 3.3.2 MONTAGE SHOWING CROSS-SECTIONAL TEM OF MESA

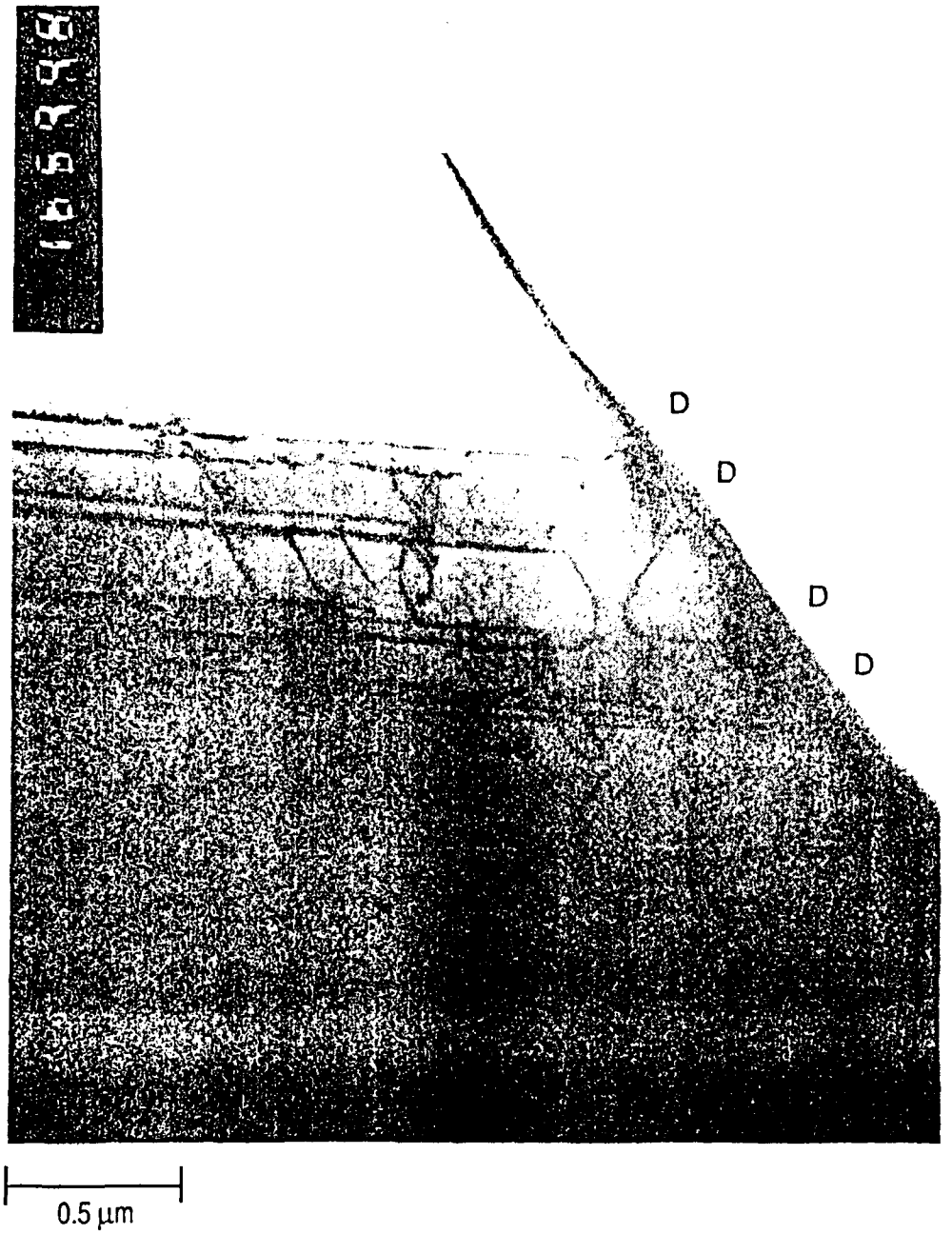
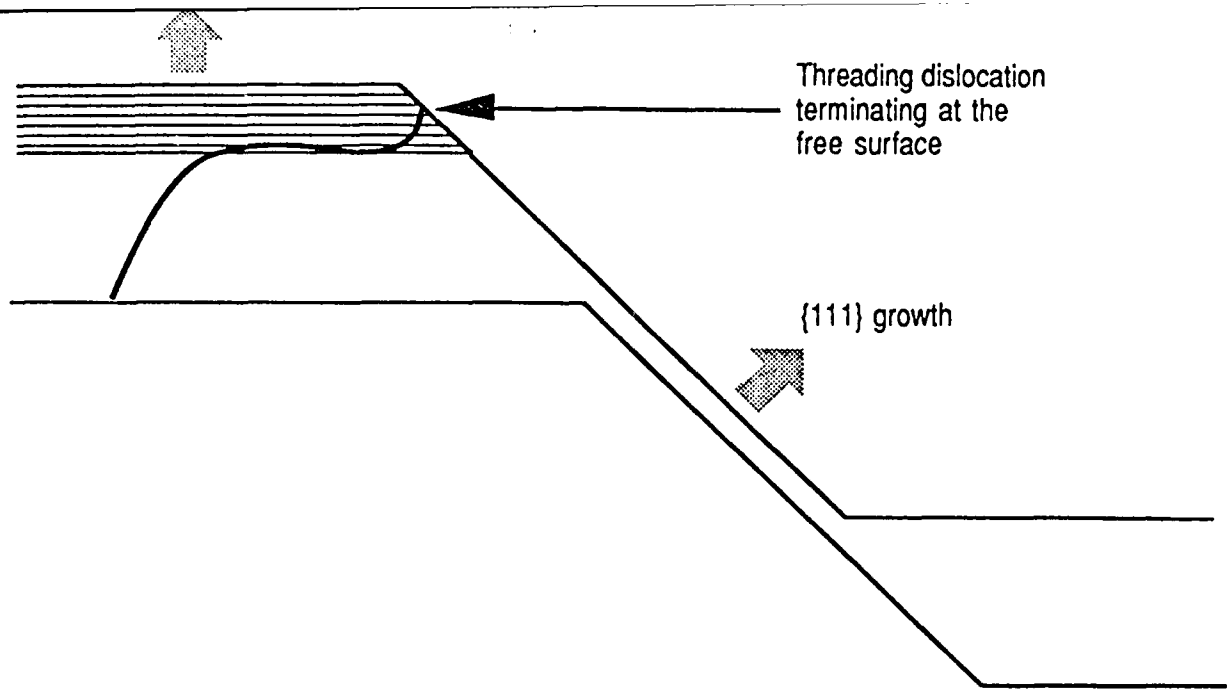
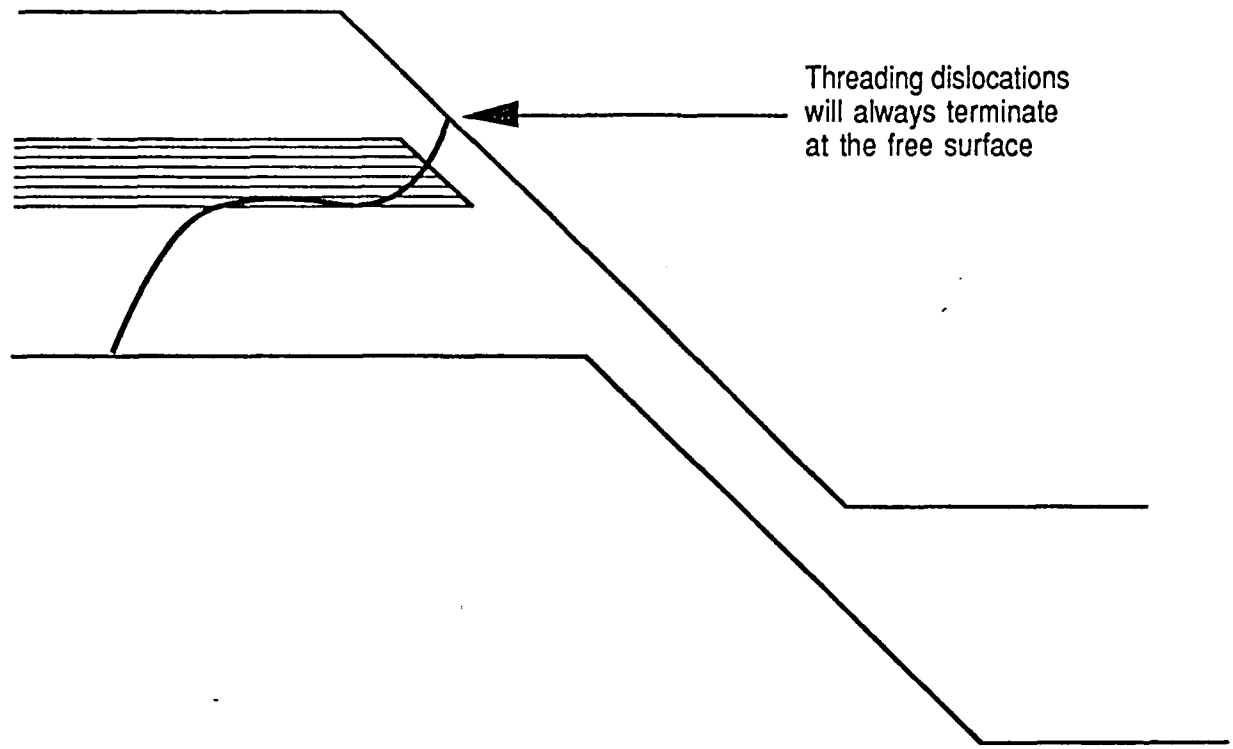


Fig 3.3.3 MESA SIDEWALL - SHOWING TERMINATION OF DEFECTS AT MESA EDGE



a) The loss of threading dislocations for the mesa edge after the growth of the first few strained layer periods



b) Showing how the threading dislocation length is always extended to reach the free surface with continued growth

Fig 3.3.4